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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,823	09/25/2003	Maximino Aguilar JR.	AUS920030707US1	7305
40412 7590 11/16/2007 IBM CORPORATION- AUSTIN (JVL) C/O VAN LEEUWEN & VAN LEEUWEN PO BOX 90609 AUSTIN, TX 78709-0609			EXAMINER JEAN GILLES, JUDE	
			ART UNIT 2143	PAPER NUMBER
			MAIL DATE 11/16/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/670,823

Applicant(s)

AGUILAR ET AL.

Examiner

Jude J. Jean-Gilles

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>See Continuation Sheet</u> . | 6) <input type="checkbox"/> Other: _____ |

Continuation of Attachment(s) 3. Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/02/2007, 07/16/2007, 05/20/2007, 03/29/2007, 01/04/2007, 10/13/2006, 09/19/2006, 08/15/2006, 05/16/2006, 11/11/2005, and 09/25/2003 .

DETAILED ACTION

This office action is responsive to communication filed on 09/25/2003.

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement submitted on 10/02/2007, 07/16/2007, 05/20/2007, 03/29/2007, 01/04/2007, 10/13/2006, 09/19/2006, 08/15/2006, 05/16/2006, 11/11/2005, and 09/25/2003 have been considered by the examiner (see attached PTO-1449A).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7, 15, and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Claims 7, 15, and 23 contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. In claim 15, and 23, Applicants claims "translating the application's instructions to secondary processor's instructions", and further in claim 7 "translating the application's instructions to secondary processor instructions using the operating system" is not described in the specifications. It has not been disclosed how such

limitation is taken place. Therefore, one skilled in the art would not know how to make and/or use the invention as claimed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office Action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-6, 8-14, 16-22, and 24** are rejected under 35 U.S.C. 102(b) as being anticipated by Kauffman et al (hereinafter Kauffman), Patent No. 6,199,179 B1.

Regarding **claim 1-6, 8-14, 16-22, and 24** Kauffman teaches:

1. A computer-implemented method for managing processors as system devices (*fig. 1, and 2*), the method comprising:

executing an operating system by one or more first processors included in a group of heterogeneous processors (*see abstract; also see fig. 13, items 1304, and 1308; column 4, lines 50-61; column 5, lines 60-65; column 8, lines 65-67, continue in column 9, lines 1-7; note that the heterogeneous processors comprised of CPUs, and memory I/O, forming a group or partition executing an OS instance*);

loading a device module corresponding to one or more secondary processors included in the group of heterogeneous processors into the operating system (*column 3, lines 60-66; note that each machine or device module consists of processors in a group of processors, memory, and I/O, and that the running applications rely on the one*

instance of the operating system; it is critically important to note that inherently, the machine modules are loaded prior to running the applications these cells)

loading an application using the operating system, the application including device-oriented instructions adapted to control the one or more of the secondary processors (see abstract; also see column 5, lines 60-65; note that the abstract discloses "the secondary CPUs then dump their processing contexts, and each invokes (loads) a migration routine to transfer their control to the new operating system instances"; the migration routine is the application that contains instructions to process control of the OS instances); and

performing the device-oriented instructions at the one or more of the secondary processors (see abstract; also see column 30, lines 53-67, continue in lines 1-19 of column 31; note the performing of the PAL MIGRATE device-oriented instruction at the secondary processors).

2. The method of claim 1, further comprising setting up a device-like access for one or more of the secondary processors, the device-like access being used by the application to access one or more of the secondary processors (see abstract; column 5, lines 60-65; the abstract specifically discloses "For CPUs, destination instance IDs are stored in an array which is accessed upon occurrence of a failure to determine where the CPUs will be assigned. The secondary CPUs then dump their processing contexts, and each invoke a migration routine to transfer their control to the new instances).

3. The method of claim 2, further comprising creating a configuration file, the configuration file containing a list of one or more of the secondary processors and the corresponding device-like access set up for the one or more secondary processors (*fig. 3, items 3000; fig. 4; column 9, lines 46-51; column 11, lines 1-26, column 20, lines 4-12; note that the configuration tree is the configuration file with the list of all primary and secondary CPUs contained in the partitions*).

4. The method of claim 3, further comprising determining for which of the one or more of the secondary processor the application's device-oriented instructions are intended (see *figs. 9A-9B; column 30 lines 53 through column 31, lines 19*).

5. The method of claim 4, wherein the determining is performed using information from the configuration file (*column 31, lines 8-37; the configuration tree represents the configuration file that contains such information*).

6. The method of claim 1, wherein the loading the device module facilitates a communication between the application and one or more of the secondary processors by extending the operating system (*column 13, lines 6-12; note that allowing the operating system to build bus and device configuration tables without probing the buses offers extended operating systems operations with additional software to provide users with application-specific work operations*).

8. The method of claim 1, wherein the performing the device-oriented instructions comprises the one or more secondary processors processing application-provided data according to the application's device-oriented instructions (*see abstract; also see column 30, lines 53-67, continue in lines 1-19 of column 31; note the performing of the PAL MIGRATE device-oriented instruction at the secondary processors*).

9. An information handling system comprising:

a plurality of heterogeneous processors, wherein the plurality of heterogeneous processors includes one or more first processors and one or more secondary processors (*see Kauffman; see abstract; also see fig. 13, items 1308, and 1304; column 4, lines 38-61; column 5, lines 60-65; note that the heterogeneous processors comprised of first or Primary processors , and secondary processors*); and

a common memory accessible by the plurality of heterogeneous processors (*see Kauffman; fig. 13, item 1310*), wherein:

the one or more first processors (*see Kauffman; see fig. 13, items 1308, and 1304*) are adapted to:

execute an operating system (*see Kauffman; see abstract; also see fig. 13, items 1304, and 1308; column 8, lines 65-67, continue in column 9, lines 1-7*);

load a device module corresponding to the one or more secondary processors into the operating system (*see Kauffman; column 3, lines 60-66; note*

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that each machine or device module consists of processors in a group of processors, memory, and I/O, and that the running applications rely on the one instance of the operating system; it is critically important to note that inherently, the machine modules are loaded prior to running the applications these cells); and

load an application using the operating system, the application including device-oriented instructions adapted to control the one or more secondary processors (see Kauffman; see abstract; also see column 5, lines 60-65; note that the abstract discloses "the secondary CPUs then dump their processing contexts, and each invokes (loads) a migration routine to transfer their control to the new operating system instances"; the migration routine is the application that contains instructions to process control of the OS instances), and

the one or more secondary processors are adapted to perform the device oriented instructions (see Kauffman; see abstract; also see column 30, lines 53-67, continue in

lines 1-19 of column 31; note the performing of the PAL MIGRATE device oriented instruction at the secondary processors).

10. The information handling system of claim 9, wherein the one or more first processors are further adapted to set up a device-like access for one or more of the secondary processors, wherein the application uses the device-like access to access one or more of the secondary processors (see Kauffman; see abstract; column 5, lines

60-65; the abstract specifically discloses "For CPUs, destination instance IDs are stored in an array which is accessed upon occurrence of a failure to determine where the CPUs will be assigned. The secondary CPUs then dump their processing contexts, and each invoke a migration routine to transfer their control to the new instances).

11. The information handling system of claim 10, wherein the one or more first processors are further adapted to create a configuration file, the configuration file containing a list of one or more of the secondary processors and the corresponding device-like access set up for the one or more secondary processors. (see Kauffman; *fig. 3, items 3000; fig. 4; column 9, lines 46-51; column 11, lines 1-26, column 20, lines 4-12; note that the configuration tree is the configuration file with the list of all primary and secondary CPUs contained in the partitions).*

12. The information handling system of claim 11, wherein the one or more first processors are further adapted to determine for which one of the secondary processors the application's device-oriented instructions are intended (see Kauffman; *see figs. 9A-9B; column 30, lines 53-27).*

13. The information handling system of claim 12, wherein the one or more first processors are adapted to perform the determining by using information from the configuration file (see Kauffman; *column 31, lines 8-37; the configuration tree represents the configuration file that contains such information).*

14. The information handling system of claim 9, wherein the one or more first processors are adapted to load the device module to facilitate a communication between the application and one or more of the secondary processors by extending the operating system (see Kauffman; *column 13, lines 6-12; note that allowing the operating system to build bus and device configuration tables without probing the buses offers extended operating systems operations with additional software to provide users with application-specific work operations*).

16. The information handling system of claim 9, wherein the one or more secondary processors are adapted to perform the instructions by the one or more secondary processors processing application-provided data according to the application's device-oriented instructions (see Kauffman; *see abstract; also see column 30, lines 53-67, continue in lines 1-19 of column 31; note the performing of the PAL MIGRATE device-oriented instruction at the secondary processors*).

17. A computer program product on computer operable media, the computer program product comprising:

means for executing an operating system by one or more first processors included in a group of heterogeneous processors (see Kauffman; *see abstract; also see fig. 13, items 1304, and 1308; column 8, lines 65-67; column 8, lines 65-67, continue in column 9, lines 1-7*);

means for loading a device module corresponding to one or more secondary processors into the operating system, wherein the secondary processors are included in the group of heterogeneous processors (see Kauffman; *column 3, lines 60-66; note that each machine or device module consists of processors in a group of processors, memory, and I/O, and that the running applications rely on the one instance of the operating system; it is critically important to note that inherently, the machine modules are loaded prior to running the applications these cells*);

means for executing an application, the application including device-oriented instructions adapted to control the one or more of the secondary processors (see Kauffman; *see abstract; also see column 5, lines 60-65; note that the abstract discloses "the secondary CPUs then dump their processing contexts, and each invokes (loads) a migration routine to transfer their control to the new operating system instances"; the migration routine is the application that contains instructions to process control of the OS instances*), and

means for performing the device-oriented instructions at the one or more of the secondary processors (see Kauffman; *see abstract; also see column 30, lines 53-67, continue in lines 1-19 of column 31; note the performing of the PAL MIGRATE device-oriented instruction at the secondary processors*).

18. The computer program product of claim 17, further comprising means for setting up a device-like access for one or more of the secondary processors, the device-like access being used by the application to access one or more of the secondary

processors (see Kauffman; *see abstract; column 5, lines 60-65; the abstract specifically discloses "For CPUs, destination instance IDs are stored in an array which is accessed upon occurrence of a failure to determine where the CPUs will be assigned. The secondary CPUs then dump their processing contexts, and each invoke a migration routine to transfer their control to the new instances).*

19. The computer program product of claim 18, further comprising means for creating a configuration file, the configuration file containing a list of one or more of the secondary processors and the corresponding device-like access determined for the one or more secondary processors (see Kauffman; *fig. 3, items 3000; fig. 4; column 9, lines 46-51; column 11, lines 1-26, column 20, lines 4-12; note that the configuration tree is the configuration file with the list of all primary and secondary CPUs contained in the partitions).*

20. The computer program product of claim 19, further comprising means for determining for which of the one or more of the secondary processor the application's device-oriented instructions are intended (see Kauffman; *see figs. 9A-9B; column 30, lines 53-27).*

21. The computer program product of claim 20, wherein the means for determining uses information from the configuration file (see Kauffman; *column 31, lines 8-37; the configuration tree represents the configuration file that contains such information).*

22. The computer program product of claim 17, wherein the means for loading the device module facilitates a communication between the application and one or more of the secondary processors (see Kauffman; *column 13, lines 6-12; note that allowing the operating system to build bus and device configuration tables without probing the buses offers extended operating systems operations with additional software to provide users with application-specific work operations*).

24. The computer program product of claim 17, wherein the means for performing the instructions comprises means for processing application-provided data according to the application's device-oriented instructions (see Kauffman; *see abstract; also see column 30, lines 53-67, continue in lines 1-19 of column 31; note the performing of the PAL MIGRATE device-oriented instruction at the secondary processors*).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 7, 15, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kauffman in view of Yamazaki (hereinafter Yama), U.S. Patent No 5,812,843.

Regarding **claim 7**, Kauffman teaches the invention substantially as claimed. Kauffman discloses method for managing processors as system devices of claim 1, but does not disclose a method comprising translating the application's instructions to secondary processor instructions using the operating system. It is important to note that this step is not enabled in the specifications as claimed and that it is examined as best understood by the examiner (*see rejection under 35 U.S.C. 112, first paragraph in page 1 of this action*)

In an analogous art, Yama shows the technique of using a translating program's instructions in order to process them in a secondary or backup processor. Yama discloses a system in which "...*If the job-executing program exists in another class, the processor converts the program and data, and transfers them to a back-end processor 7 running under a different operating system, to request execution. After receiving the execution results, the first processor executes the processing. The front-end processor 1 consists of a job entry unit 2, a language conversion/transfer unit 3, a data conversion/transfer unit 4, and a job invocation unit 5...*" (see Yama; column 1, lines 51-59; see also figs. 1, and 5). Further in lines 43-49 of column 3, Yama teaches "*There are classified two types of job class: one is a class for executing the job under UXP, which is the operating system running on the back-end processor 7, and the other is a class for executing the*

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job under MSP, which is the operating system running on the front-end processor...".

In an attempt to facilitate operations between the processors, the Operating system through the program and data conversion unit is capable of executing an interconnection program to transfer the converted code from the front-end processor to the back-end processor (see *Yama*, *fig. 2*, also see *column 4, line 13-24*).

Accordingly, it would have been obvious to one of ordinary skill in the networking art at the time the invention was made to have incorporated Yama's teachings of a system of translating the application's instructions to secondary processor instructions with the teachings of Kauffman, for the purpose of permitting "...*automatic program and data conversion thereby allowing the user to take advantage of the secondary processor without being conscious of the differences between programming languages ...*" as stated by Yama in lines 40-55 of column 13. By this rationale **claim 7** is rejected.

15. The information handling system of claim 9, wherein the one or more first processors are adapted to facilitate a communication between the application and one or more of the secondary processors device-oriented instructions by translating the application's instructions to secondary processor's instructions (see *Yama*; *column 1, lines 51-59; column 4, line 13-24; see also figs. 1, 2, and 5*). The same motivation and reason to combine that were utilized for the rejection of claim 7 are also valid for this claim. By this rationale, **claim 15** is rejected.

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23. The computer program product of claim 17, further comprising means for translating the application's instructions to secondary processor instructions (*see Yama; column 1, lines 51-59; column 4, line 13-24; see also figs. 1, 2, and 5*). The same motivation and reason to combine that were utilized for the rejection of claim 7 are also valid for this claim. By this rationale, **claim 23** is rejected.

Conclusion

7. **THIS ACTION IS MADE NON-FINAL.** Any inquiry concerning this communication or earlier communications from examiner should be directed to Jude Jean-Gilles whose telephone number is (571) 272-3914. The examiner can normally be reached on Monday-Thursday and every other Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley, can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3201.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-0800.

Jude Jean-Gilles

Patent Examiner

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JJG

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23. The computer program product of claim 17, further comprising means for translating the application's instructions to secondary processor instructions (*see Yama; column 1, lines 51-59; column 4, line 13-24; see also figs. 1, 2, and 5*). The same motivation and reason to combine that were utilized for the rejection of claim 7 are also valid for this claim. By this rationale, **claim 23** is rejected.

Conclusion

7. **THIS ACTION IS MADE NON-FINAL.** Any inquiry concerning this communication or earlier communications from examiner should be directed to Jude Jean-Gilles whose telephone number is (571) 272-3914. The examiner can normally be reached on Monday-Thursday and every other Friday from 8:00 AM to 5:30 PM.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-0800.

Jude Jean-Gilles

Patent Examiner

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JJG

November 11, 2007

A handwritten signature in black ink, appearing to read 'J. Gilles', is written over the printed name and title of the examiner.